CEM3407L

Dual P-Channel Enhancement Mode Field Effect Transistor

FEATURES

■ -30V, -5.1A, $R_{DS(ON)}$ = 48mΩ @V_{GS} = -10V.

$R_{DS(ON)}$ = 65mΩ @V_{GS} = -4.5V.

$R_{DS(ON)}$ = 115mΩ @V_{GS} = -2.5V.

■ Super high dense cell design for extremely low $R_{DS(ON)}$.

■ High power and current handing capability.

■ Lead free product is acquired.

■ Surface mount Package.

SO-8

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D1 8 D1 7 D2 6 D2 5

S1 1 G1 2 S2 3 G2 4
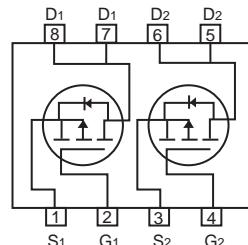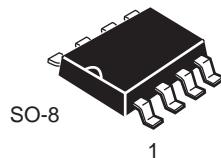
ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±12	V
Drain Current-Continuous	I_D	-5.1	A
Drain Current-Pulsed [a]	I_{DM}	-20.4	A
Maximum Power Dissipation	P_D	2.0	W
Operating and Store Temperature Range	T_J, T_{stg}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Ambient [b]	$R_{θJA}$	62.5	°C/W

Electrical Characteristics T_A = 25$°$C unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V			-1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	V_{GS} = 12V, V_{DS} = 0V			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	V_{GS} = -12V, V_{DS} = 0V			-100	nA
On Characteristics [c]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = -250μA	-0.6		-1.4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -5.1A		40	48	mΩ
		V_{GS} = -4.5V, I_D = -4.6A		50	65	mΩ
		V_{GS} = -2.5V, I_D = -3.7A		85	115	mΩ
Dynamic Characteristics [d]						
Input Capacitance	C_{iss}	V_{DS} = -15V, V_{GS} = 0V, f = 1.0 MHz		905		pF
Output Capacitance	C_{oss}			200		pF
Reverse Transfer Capacitance	C_{rss}			160		pF
Switching Characteristics [d]						
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D= -5.1A, V_{GS} = -10V, R_{GEN} = 6Ω		10	20	ns
Turn-On Rise Time	t_r			4	8	ns
Turn-Off Delay Time	$t_{d(off)}$			40	80	ns
Turn-Off Fall Time	t_f			5	10	ns
Total Gate Charge	Q_g	V_{DS} = -15V, I_D = -5.1A, V_{GS} = -4.5V		8.5	11	nC
Gate-Source Charge	Q_{gs}			2.5		nC
Gate-Drain Charge	Q_{gd}			1.5		nC
Drain-Source Diode Characteristics and Maximun Ratings						
Drain-Source Diode Forward Current [b]	I_S				-2	A
Drain-Source Diode Forward Voltage [c]	V_{SD}	V_{GS} = 0V, I_S = -1A			-1	V

Notes :
a.Repetitive Rating : Pulse width limited by maximum junction temperature.
b.Surface Mounted on FR4 Board, t < 5 sec.
c.Pulse Test : Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
d.Guaranteed by design, not subject to production testing.
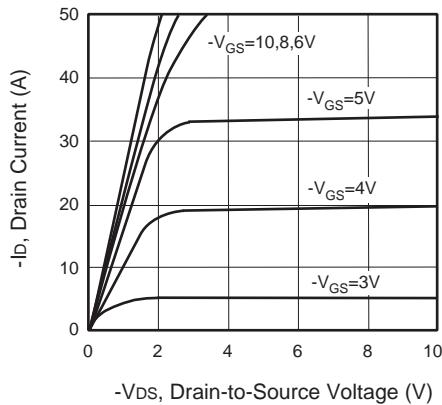
Figure 1. Output Characteristics
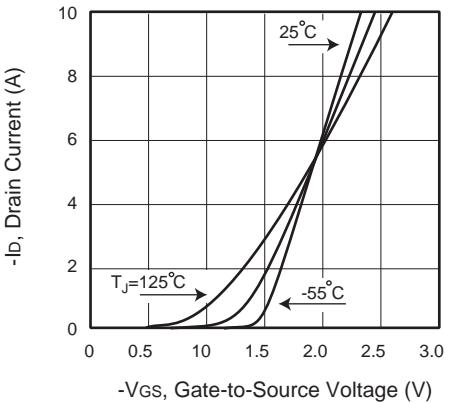
**Figure 2. Transfer Characteristics**
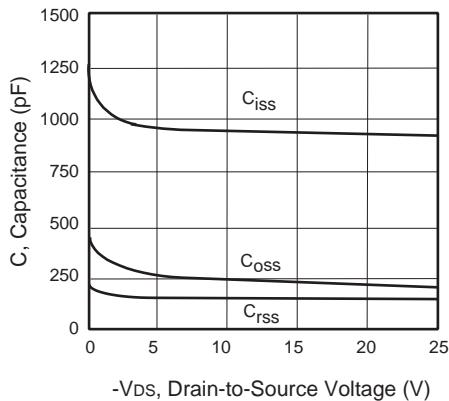
Figure 3. Capacitance
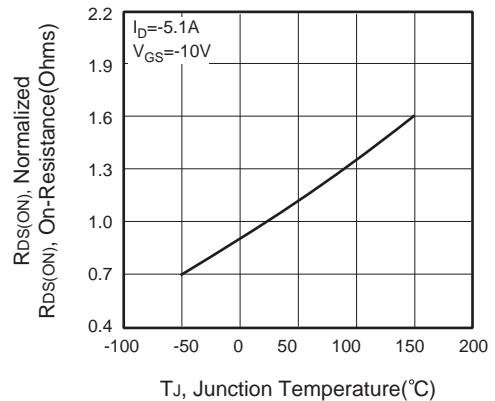
Figure 4. On-Resistance Variation with Temperature
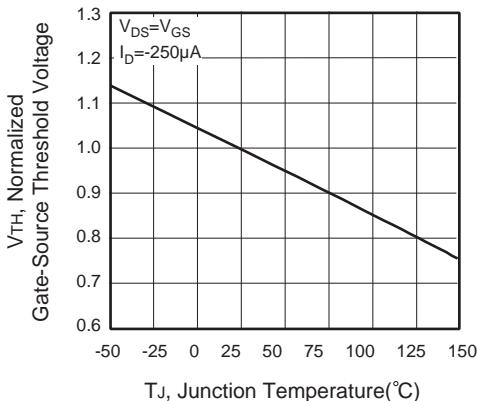
Figure 5. Gate Threshold Variation with Temperature
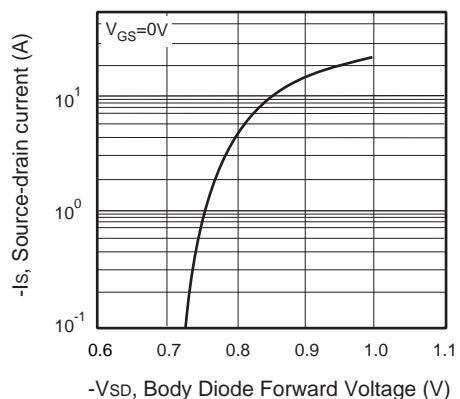
**Figure 6. Body Diode Forward Voltage Variation with Source Current**
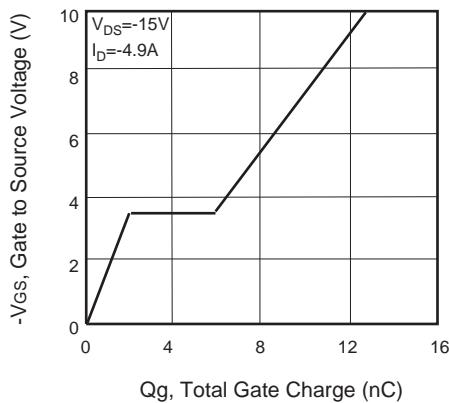
**Figure 7. Gate Charge**
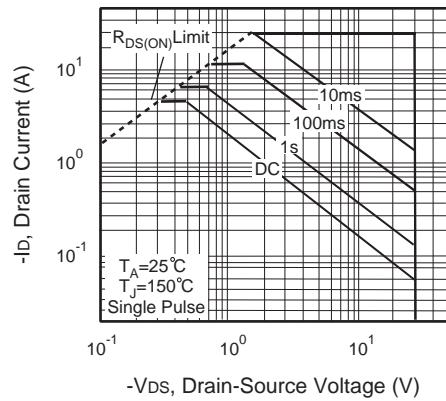
Figure 8. Maximum Safe Operating Area
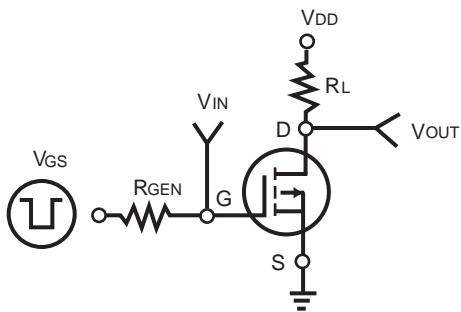
Figure 9. Switching Test Circuit
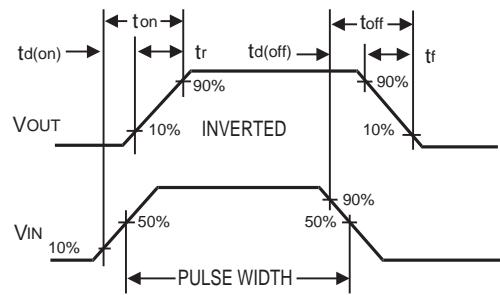
Figure 10. Switching Waveforms

1. $R_{JA}(t) = r(t) * R_{JA}$
2. R_{JA} = See Datasheet
3. $T_{JM}-T_A = P * R_{JA}(t)$
4. Duty Cycle, D=t1/t2
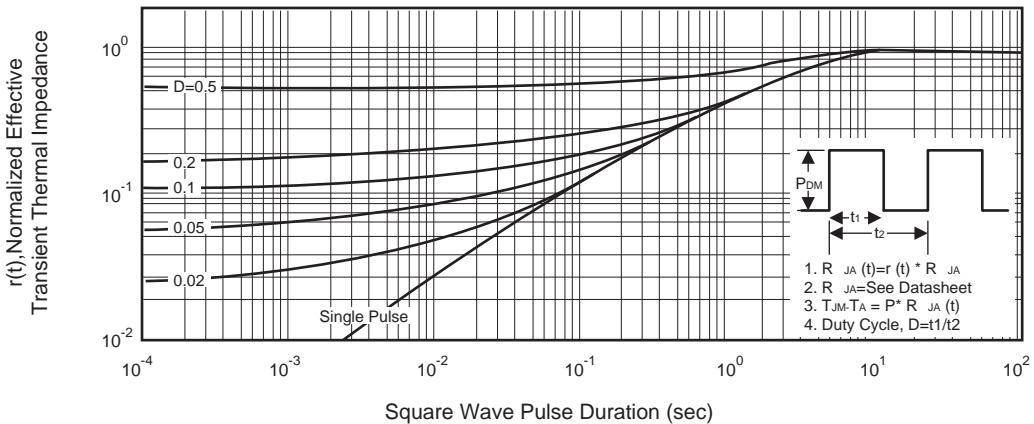
Figure 11. Normalized Thermal Transient Impedance Curve